Communications and Data Processing

UPN 310-20-08

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Semi-Annual Review of the FY97 SOMO/MO&DSD Technology Development Program

April 15, 1997

Communications and Data Processing
Objective and Significance

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Overall Objective

Dramatically reduce the cost of high rate earth and space science data acquisition and first level processing.

Goals	Significance
#1: Demonstrate high performance (over 150Mbps) baseband CCSDS return link telemetry gateway (F/S, R/S, Packet Proc) which can be reproduced at less than $25K cost. Develop card to plug directly into PC or standard (PCI based) workstation.	• **Dramatically reduce the size and cost of acquiring and processig CCSDS telemetry for missions such as EOS, L7, SpaceStation, SMEX, MIDEX, New Millenium. Transfer technology to industry as it is developed.**
#2: Design high performance (over 300Mbps BPSK, QPSK) , low cost single chip parallel digital reciever ASIC. Incorporate onto board which includes high performance Viterbi decoding and bit sync functions.	• **Low cost PC based CCSDS telemetry systems capable of recieving data at rates over 300Mbps are made possible for reproduction costs under $25K.**

April 15, 1997

Communications and Data Processing
Products and Customers

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Product	Goal #	User/Customer	Development Phase				Approach/Comments
			Concept	Design	Demo	Transfer	
VLSI Comm G/W	1	EOS SMEX, ESDIS,GN		■			Completed Phase 1, high commercial interest.
Parallel Integrated F/S Chip	1	EOS, SMEX, MIDEX , GN				■	Multi-satellite formats, Operation to 550Mbps. High commercial interest.
Service Processor ASIC	1	EOS, SMEX, MIDEX , GN			■		Highly programmable, 1million packets/sec. High commercial interest
PCI10FR Board	1	EOS, SMEX, MIDEX , GN				■	PCI based board,fwd and return link frame processing up to 15Mbps. Commercialization in process.
Return Link Proc Board	1	EOS, SMEX, MIDEX , GN			■		Full return link processing up to 150Mbps in PC/Workstation compatible board. Frame and packet level processing. Prototype board received and working.
HR CMOS Digital Rcvr ASIC	2	EOS, TDRSS, GN, SN		■			Single chip BPSK and QPSK receiver. Operation to 150Mbps per channel.
PCI Receiver Board	2	EOS, TDRSS, GN, SN	■				PCI Receiver Board, Operation to 300Mbps PC or Workstation

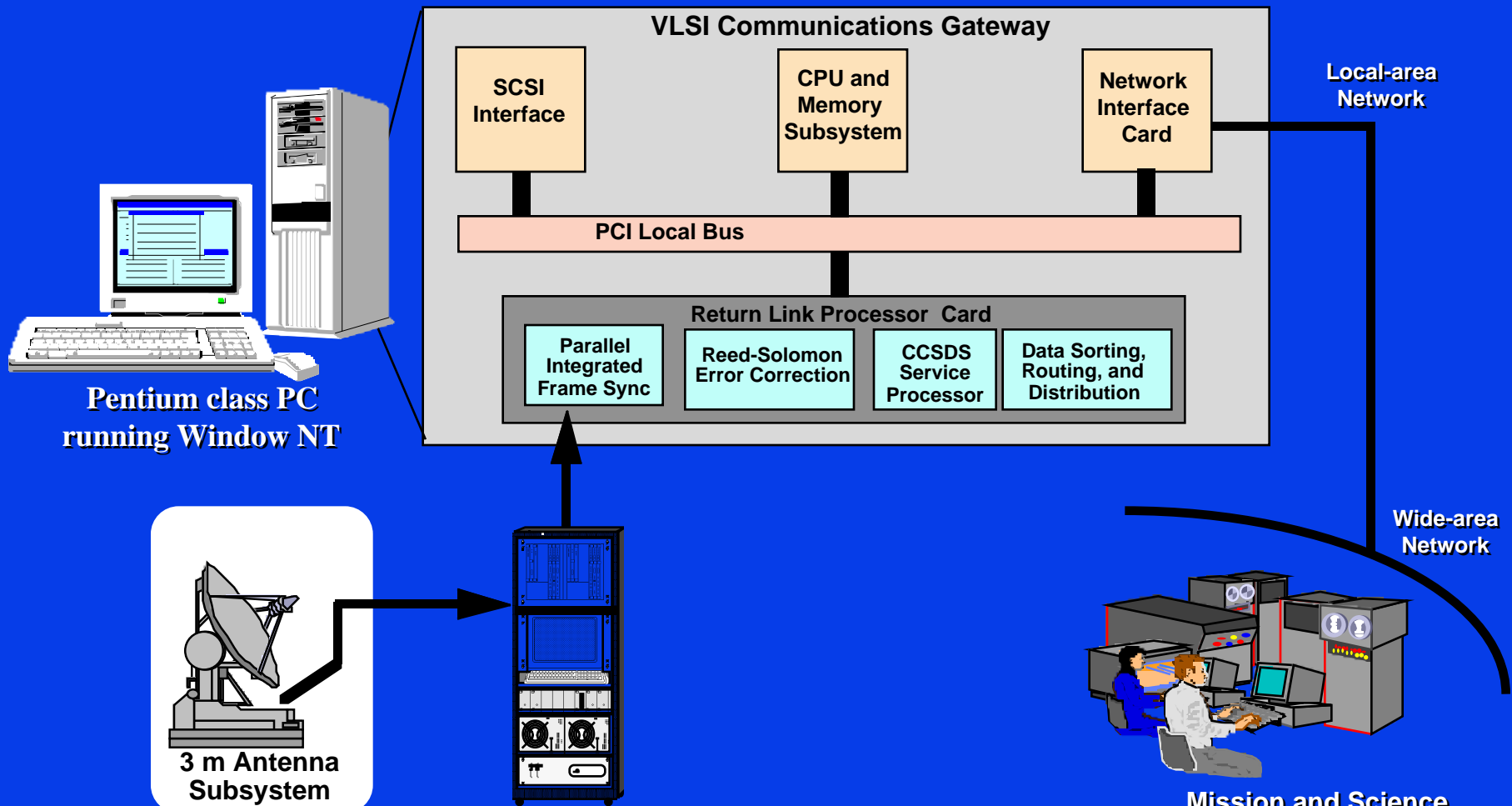FY97 SOMO/MO&DSD Technology Development Program Semi-Annual Review

Communications and Data Processing
Goal #1 FY97 Accomplishments

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Demonstrate high rate (150 Mbps) baseband CCSDS Return Link Communication Gateway System (Goal #1)

VLSI Communications Gateway

SCSI Interface	CPU and Memory Subsystem	Network Interface Card

Local-area Network

PCI Local Bus

Return Link Processor Card

Parallel Integrated Frame Sync	Reed-Solomon Error Correction	CCSDS Service Processor	Data Sorting, Routing, and Distribution

Pentium class PC running Window NT

3 m Antenna Subsystem

Wide-area Network

Mission and Science Operation Center

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Goal #1 FY97 Accomplishments (cont'd)

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- **Completed fabrication of Service Processor ASIC:**
  - **Single chip, 0.4 μ CMOS chip performs packet/frame processing and maintains full data quality and accounting information.**
  - **Highly programmable, handles all standard CCSDS AOS return link services including packet extraction and reassembly.**
  - **Will operate at nominal packet rates over 1 million packets/sec and data rates to 300 Mbps.**
  - **High commercial interest. Two companies interested in receiving prototypes.**
  - **Patent application in process, cost in quantity, $350 per chip.**

- **Began technology transfer of PCI10FR board which incorporates PIFS and R/S Error Correction Chips:**
  - **Operating at return link rates up to 15Mbps. Also performs command uplink interface functions.**
  - **High commercial interest, multiple projects interested in utilizing board SMEX, TOMS, GN (Wallops), ESDIS (Regional Data Centers). Lockheed Martin interested in commercializing card.**
  - **Currently available for Technology Transfer.**

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Parallel Digital Receiver Board Specifications

Input:
Up to 150Mbps differential serial ECL
Functions:
Frame Synchronization, Reed-Solomon Error Correction (225,256), CCSDS Service Processing (VCDU, Packet,VCA, Insert, Pass thru)
High Rate DMA via PCI bus transfer
Full Data Quality Accounting
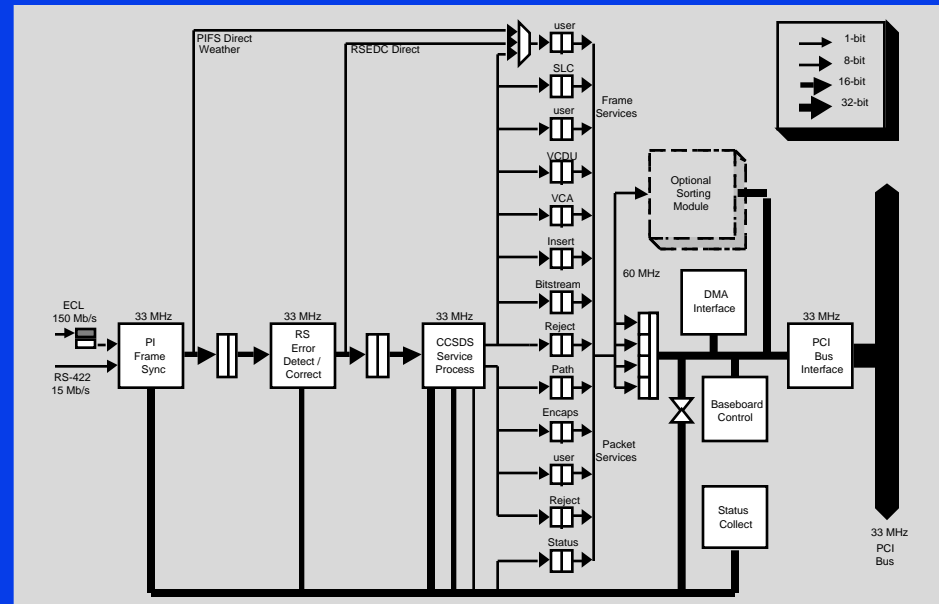**Performance**:
100Kpackets /sec(worst case)
to 1Mpackets/sec (best case)
100K frames per second
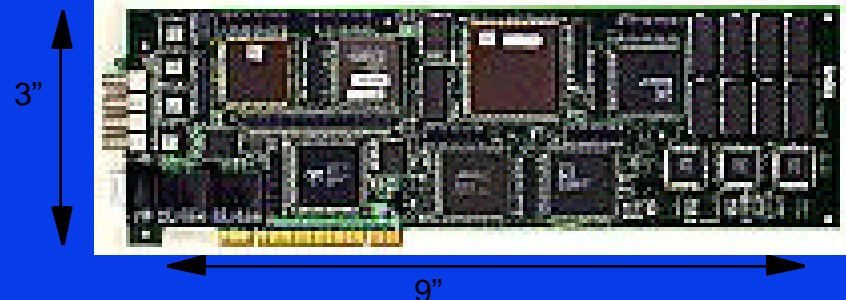*64 virtual channels*
2048 application id's

Return Link Processor Card Block Diagram

Development Status

- **CDR was held in early November 1996.**

- **Completed fabrication in January 1997.**

- **Testing board in Gateway 2000 PC and Dec Alpha 2100A workstation**

- **Successfully tested PIFS, RSEC, and Service Processor chips at rates up to 180Mbps with 300,000 packets per second**
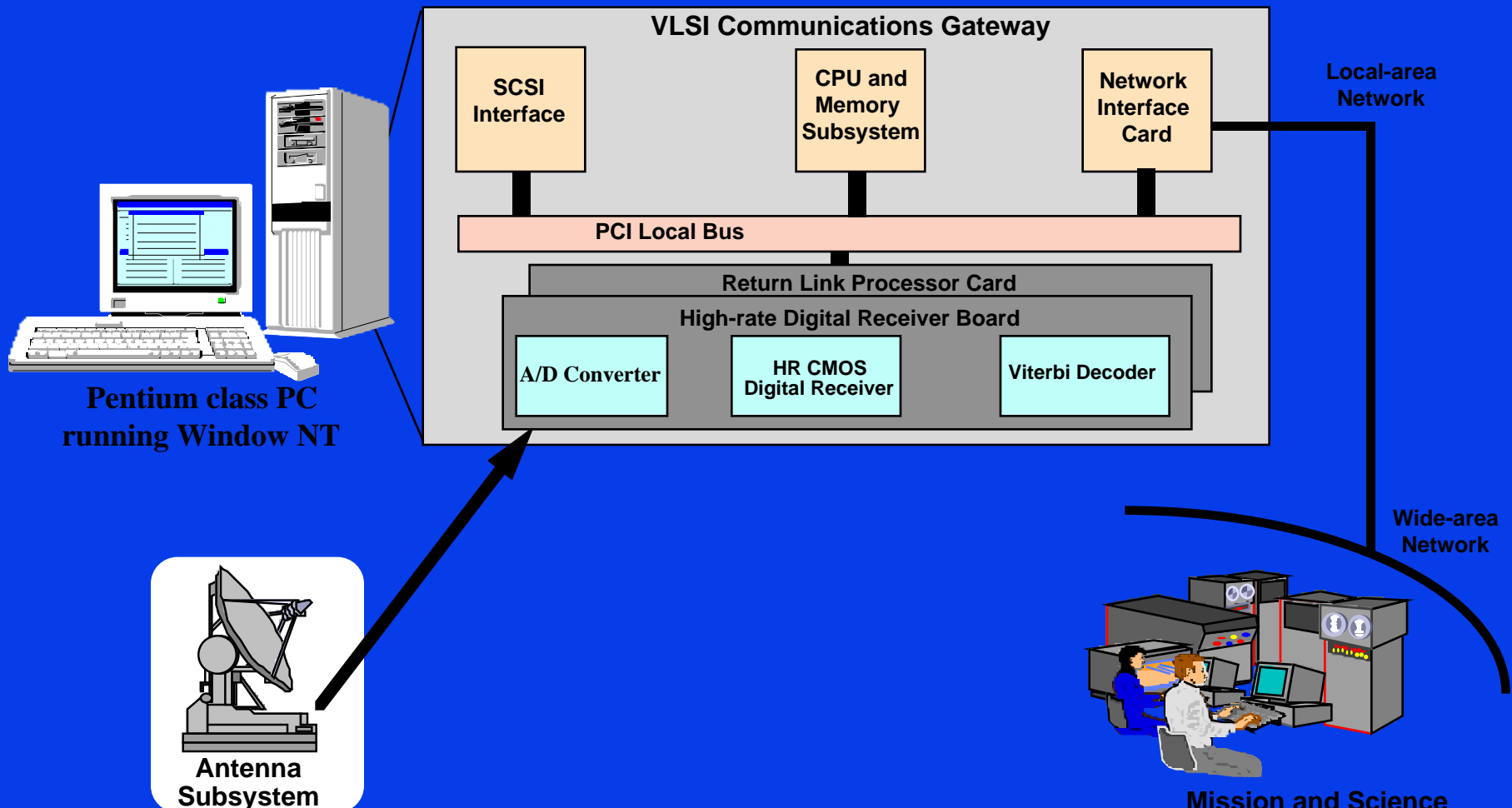
RLPC Board

3"

9"

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Goal #2 FY97 Accomplishments

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Develop high rate Parallel Digital Receiver ASIC and PC compatible board (Goal #2)

Pentium class PC running Window NT

VLSI Communications Gateway

| SCSI Interface | CPU and Memory Subsystem | Network Interface Card |

Local-area Network

PCI Local Bus

Return Link Processor Card

High-rate Digital Receiver Board

| A/D Converter | HR CMOS Digital Receiver | Viterbi Decoder |

Wide-area Network

Antenna Subsystem

Mission and Science Operation Center

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Goal #2 FY97 Accomplishments (cont'd)

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High Rate Digital Receiver Board Specifications

Input:
Down converted BPSK or QPSK signal at rates up to 1.4G sym/sec
Functions:
Parallel digital receiver, BPSK or QPSK demodulation, Viterbi rate 1/2, constraint length 7 decoding
Bit synchronization
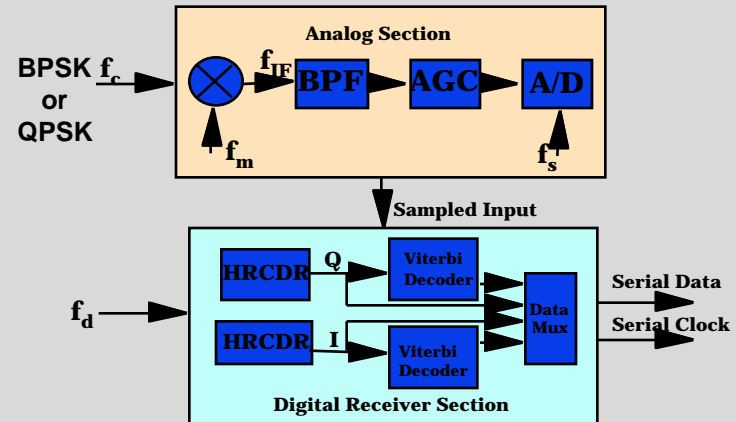**Performance**:
150Mbps per channel (I and Q)
Costs:
$350 per chip
$5k per board (reproduction cost)

Development Status

- **Defined initial architecture with JPL.**

- **Conducted PDR for FPGA implementation in March 1997.**

High Rate Digital Receiver Board Block Diagram

Development Approach

- **Phase I - Prototype Digital Receiver architecture using FPGA implementation on 9U VME boards. Tune the architecture before moving to ASIC implementation. Target date June 97.**

- **Phase II - submicron CMOS ASIC design, single channel BPSK or QPSK operation at rates up to 300Mbps. Target design complete Feb 98.**

- **Phase III - advanced modulation, higher data rates (up to 600 Mbps).**

TELECOMMUNICATIONS AND MISSION OPERATIONS
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Goal #2 FY97 Accomplishments (cont'd)

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FY97 Scorecard

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✓ **Transfer PC10FR board which performs frame synchronization and R/S error correction to commercial industry (Goal #1).**

✓ **Perform CDR and fabrication of Service Processor ASIC. Transfer prototypes to commercial industry (Goal #1).**

●●● **Test Service Processor ASIC and verify operation at rates up to 300Mbps and 250k packets/ sec (Goal #1).**

✓ **Integrate PIFS, RSEC and Service Processor ASIC on RLPC board. Fabricate the RLPC board (Goal #1).**

●●● **Test RLPC board and verify system operations in PC/Workstation at rates up to 150Mbps (Goal #1).**

●●● **Demonstrate high rate baseband CCSDS gateway system in PC and workstation, show operation at 150Mbps (Goal #1).**

●●● **Transfer RLPC board to commercial industry (Goal #1).**

✓ **Collaboratively developed initial architecture for parallel digital receiver architecture which will be initially implemented in FPGA devices (Goal #2).**

●●● **Prototype High-rate CMOS Digital Receiver architecture in FPGA devices (Goal #2).**

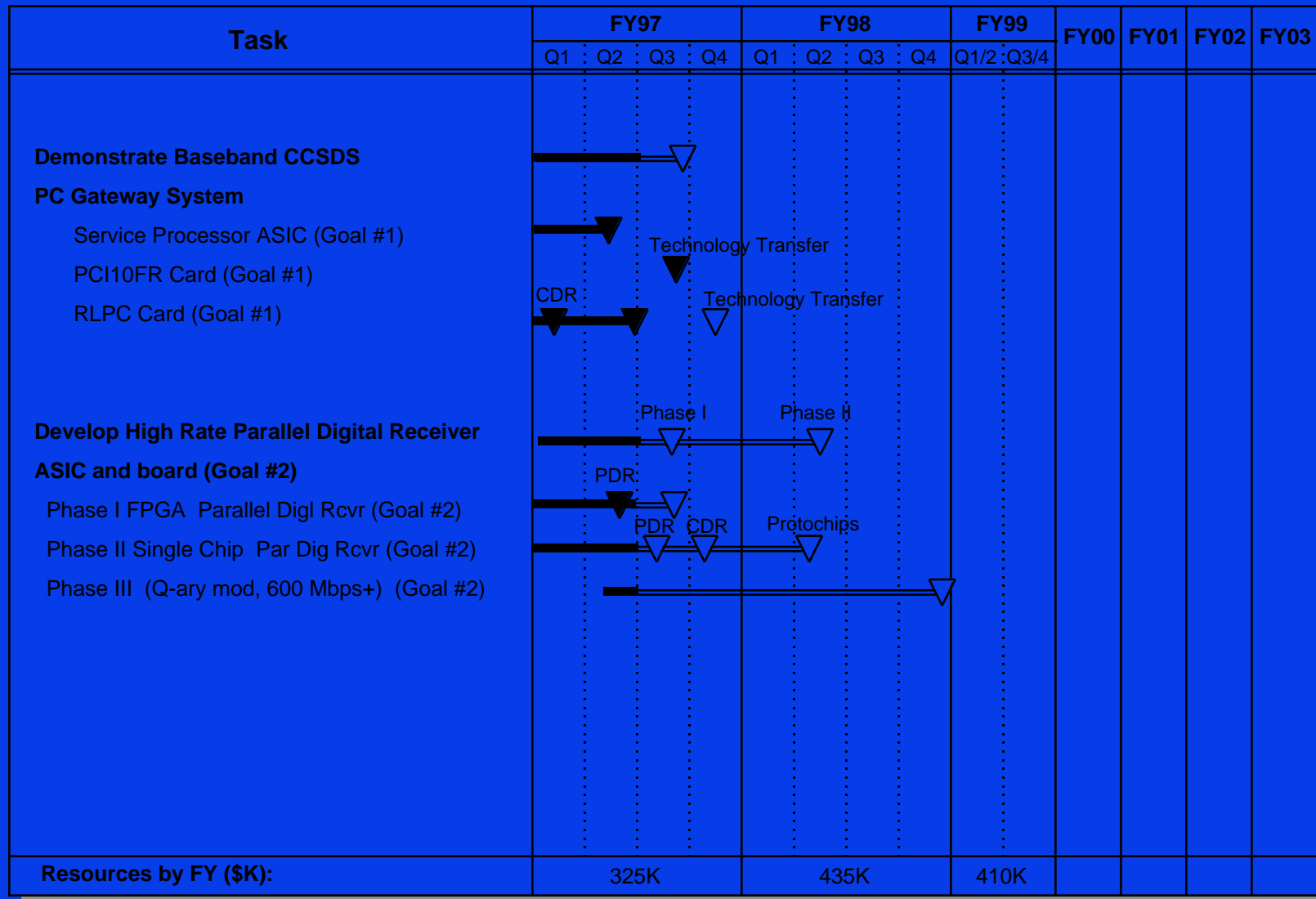# Communications and Data Processing
FY98 Goals

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- **Complete design of High-rate Digital Receiver ASIC (Goal #2).**

- **Complete development of PC/workstation compatible High-rate Digital Receiver board (Goal #2).**

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Schedule

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Task	FY97				FY98				FY99		FY00	FY01	FY02	FY03
	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1/2	Q3/4				

Demonstrate Baseband CCSDS

PC Gateway System

   Service Processor ASIC (Goal #1)

   PCI10FR Card (Goal #1) — Technology Transfer

   RLPC Card (Goal #1) — CDR — Technology Transfer

Develop High Rate Parallel Digital Receiver

ASIC and board (Goal #2) — Phase I — Phase II

 Phase I FPGA Parallel Digl Rcvr (Goal #2) — PDR

 Phase II Single Chip Par Dig Rcvr (Goal #2) — PDR CDR Protochips

 Phase III (Q-ary mod, 600 Mbps+) (Goal #2)

| Resources by FY ($K): | 325K | | | | 435K | | | | 410K | | | | | |

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Issues

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- **Funding for building the High-rate CMOS Digital Receiver ASIC.**
  - manpower for the design and simulation of the ASIC is covered.
  - currently there are no funds in budget for the fabrication of the chip.